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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,785	10/01/2003	Kuo-Chun Wu	M-12980 US	9582

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EXAMINER	
NGUYEN, GEORGE BINH MINH	
ART UNIT	**PAPER NUMBER**
3723	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,785	WU ET AL.	
	Examiner	Art Unit	
	George Nguyen	3723	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 27 September 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 10-17 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 and 18-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of Applicant's election of Group I invention of claims 1-9 and 18-20.

Claims 10-17 were withdrawn from further consideration.

Claims 1-9 and 18-20 are presented for examination.

This application has been filed with formal drawings which are acceptable by the examiner.

Election/Restrictions

Applicant's election without traverse of Group I invention of claims 1-9 and 18-20 in the reply filed on September 27, 2004 is acknowledged. Please note that the examiner believes that there was a typo error in the election regarding to the elected claims 1-19 and 18-20 as indicated per applicant. The corrected elected claim should have been 1-9 and 18-20.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joslyn et al.'6,203,404 in view of Williams'6,549,542.

With reference to Figures 3-4, col. 2 , line 51 to col. 4, line 22, Joslyn discloses the claimed invention except for specifically batch processing a plurality of workpieces.

FIG. 2 illustrates an exemplary workpiece **25** to be chemically mechanically polished. Such comprises a bulk monocrystalline silicon substrate region **26** having a series of three field effect transistor gate lines **28** formed thereover. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive material such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductor material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrate describes above.

Workpiece **25** includes a dielectric region **30** to be polished. Region **30** might comprise, by way of example only, doped or undoped oxides, such as borophosphosilicate glass or undoped oxide deposited by decomposition of tetraethylorthosilicate (TEOS). In this example, dielectric region **30** has a nonplanar topography and a thickness "t" ultimately desired to be removed by some polishing action prior to moving the workpiece onto a subsequent nonpolishing processing step. Workpiece **25** constitutes but only one exemplary workpiece, with essentially any other workpiece being usable in accordance with the invention as claimed.

Referring to FIG. 3, dielectric region **30** on workpiece **25** is chemical mechanical polished using a first slurry in what is designated as a first chemical mechanical polishing to leave a thickness "t_1" of region **30** of the dielectric material remaining to be removed in a desired subsequent polishing removal process. Preferably, t_1 is at least 15%, and more

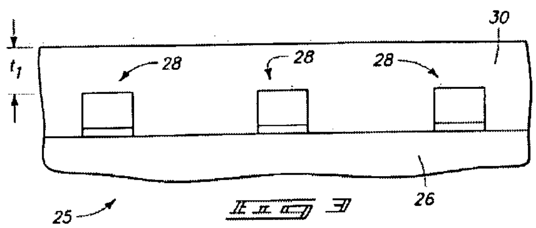


FIG. 3

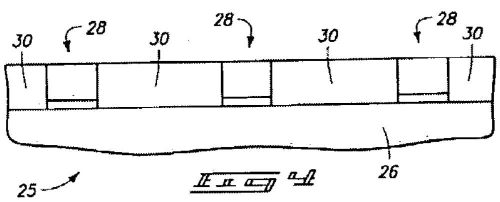


FIG. 4

preferably at least 20%, of thickness t. Further preferably, the amount of thickness t of dielectric material **30** removed to achieve t_1 preferably comprises no more than about 75% of thickness t.

Referring to FIG. **4**, dielectric region **30** is chemical mechanical polished on workpiece **25** using a second slurry different from the first slurry, and is referred to as a second chemical mechanical polishing of dielectric region **30**. The second chemical mechanical polishing comprises one or both of removal of at least 15% of thickness t or polishing with the same pad used in the first chemical mechanical polishing. Accordingly, the invention contemplates doing both, using different polishing pads but where the second chemical mechanical polishing removes at least 15% of the thickness, or using the same pad but removing less than 15% of the thickness. The depicted example shows polishing of region **30** to a point of stopping proximate outer surfaces of conductive gate lines **28**, although the invention is of course not so limited. Other workpieces might be utilized and other stopping points (defined by time, layers, etc. or combinations thereof) could be used. Further, dielectric region **30** might constitute one or more dielectric or other materials. Further, this illustrated preferred example depicts a chemical mechanical polishing method wherein the only chemical mechanical polishing of the thickness of the dielectric region being removed prior to moving the workpiece on to a subsequent nonpolishing processing step are the first and second chemical mechanical polishings. Alternately but less preferred, a third or more subsequent chemical mechanical polishing(s) might be conducted.

A preferred difference between the first and second slurries preferably relates to the aggressiveness or selective nature with which the slurries under an otherwise common set of polishing parameters remove material of region **30**. Preferably, the first slurry is chosen or designed to remove dielectric material of region **30** at a greater rate than does the second slurry under an otherwise common set of polishing parameters. In this manner in the preferred embodiment only, the first chemical mechanical polishing is conducted to be more aggressive and achieve greater inherent planarity during the first chemical mechanical polishing than would otherwise occur were the second slurry utilized initially in the first polishing under a same common set of parameters. Thereby, an advantage can be achieved in arriving at greater planarity initially, with the second polish being chosen to be more selective and less aggressive in removing material of the dielectric region. A more aggressive first polishing might have a tendency to leave a scratchy and rougher outer surface than would be desired at the conclusion of the polishing. Yet, greater overall planarity might be achieved in the combination polishing, with the second chemical mechanical polishing using a less aggressive slurry resulting in a smoother, more acceptable outer surface at the conclusion of such polish.

In a preferred embodiment, the first chemical mechanical polishing is conducted to remove dielectric material of the first region at a faster rate than during the second polishing. The first and second polishings can be conducted utilizing the same common set of polishing parameters, other than slurry composition, or using different sets of parameters. Example polishing parameters include ambient temperature, pressure, rotational and translational speeds and movements of the pad and wafer relative to one another, and pressure applied between the pad and the wafer during polishing.

The first and second slurries might differ from one another in one or more numbers of ways. For example, particles in the first slurry might differ in average size from particles in

the second slurry. The first slurry might have particles which on average are larger in size than particles in the second slurry in an effort to achieve more non-selective, aggressive removal under an otherwise common set of polishing parameters. For example, a specific average particle size for the first stated chemical mechanical polishing might constitute 120 nm, where an average particle size for the second slurry might constitute 15 nm. Further, the particles in the first slurry might differ in composition from particles in the second slurry. For example, the particles in the first slurry might on average be harder than particles in the second slurry to achieve a more aggressive, faster rate, non-selective polish in the first polishing for an otherwise common set of polishing parameters than in the second polishing. For example, the first slurry might use silica (SiO_2) particles, while softer ceria particles might be used in a second slurry. Further, the particles in the first and second slurries might differ in both size and composition. Smaller and/or softer particles in the second slurry might facilitate formation of a smoother finished outer surface at the conclusion of the polishing. Further, the particles might differ in shape, or in other manners.

Please note that in col. 4, lines 15-23, Joslyn discloses the 1st slurry is silica particles while the 2nd slurry is ceria particles.

With reference to Figure 1, col. 6, line 16 to col. 7, line 20, Williams'549 discloses a batch CMP processing of wafer with end point detection utilizing optical sensor to measure thin film thickness. Other end point detection sensors include polishing pressure and relative velocity between wafer and polishing pad.

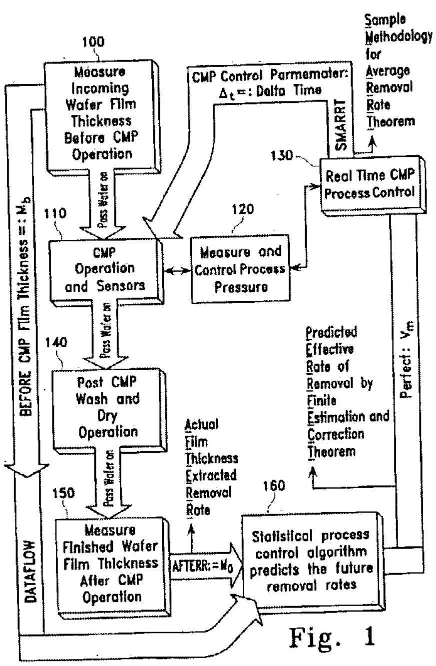


Fig. 1

Prior to polishing a wafer, a "before" thickness of the wafer is measured (**100**). More particularly, in the preferred embodiment, a thin film measurement is made on the wafer, of a layer to be polished. Such measurement may be performed by a number of available devices, such as a white light interferometer provided by Tencor of Milpitas, Calif. Another acceptable device is produced by Nova Instruments of Israel. FIG. **6** schematically illustrates a thickness measurement device (**300**) used both before and after polishing with an exemplary CMP polishing apparatus (**200**), to measure a film thickness of wafer (**102**). As noted, the CMP polishing device is merely one example of a CMP polisher for use in the present invention, and is disclosed in application Ser. No. 08/443,956 in detail, as are other embodiments. Nor is the present invention limited to only those embodiments disclosed in application Ser. No. 08/443,956, but may be applied to CMP polishers in general, and particularly those for with which the pressure between the wafer and polishing pad, the relative velocity between the wafer and the polishing pad, and the contact are of the wafer with the polishing pad are held substantially constant.

After making a thickness measurement on the wafer (**102**) to be polished, the wafer is mounted in a carrier (**101**) and applied to a polishing surface (**206**) (see FIG. **1**, (**110**)) for polishing the face of the wafer (**102**). The wafer (**102**) is polished for a predetermined time designed to remove a predetermined thickness off the face of the wafer (**102**). During polishing, the pressure applied by the wafer (**102**) against the polishing surface (**206**) is measured and controlled (**120**) through sensors which are provided on the polishing apparatus (**200**). Pressure control is preferably done in real time (**130**) using a microprocessor arrangement with feedback control over a Z-direction driver (**213**), such as that disclosed in application Ser. No. 08/443,956, for example.

After completion of the polishing of wafer (**102**), the wafer is washed and dried (**140**), and an "after polishing" thickness measurement (**150**) of the wafer (**102**) is performed using thickness measurement device (**300**). Both the "before" and "after" thickness measurements of the wafer (**102**) are compared to determine the material thickness removed and the material removal rate, as described below. These values are then used to alter the processing parameters, preferably the polishing time, of the next wafer to be polished with the goal of removing the same thickness of material from the next wafer. In the preferred embodiment, inputs from up to ten previous wafers can be considered in determining a factor by which to alter the polishing time of a subsequent wafer to be polished.

The use of a predicted CMP sequence correction polynomial (functions below) generate coefficients for an N^{th} order

linear correction method from sampled sequences. The predicted CMP sequence characterization polynomial and compensation technique is composed of two parts:

1. Actual Film Thickness Existential Removal Rate (AFTERR); and
2. Predicted CMP sequence Characterization; the Predicted Effective Rate of Removal by Finite Estimation and Correction Theory. (PERRFECT) characterization.

Depending on peculiarities common to a particular yielded manufacturers' polishing pad media, a combination of various process priming techniques are used to start a lot-size batch process that will exemplify the polishing system irregularities. This process priming technique allows the PERRFECT characterization to mathematically describe the difference between the first, semiconductor film thickness before the chemical mechanical polishing operation then second, the semiconductor film thickness after the chemical mechanical polishing operation as the actual removal rate, AFTERR, of the system. Polishing system media irregularities are subsequently tracked and the corresponding information is characterized by the PERRFECT polynomial.

As noted above, the "Material Removal Rate" is defined by subtracting the previously processed wafer's actual material film thickness from the wafer material thickness measured before polishing (i.e. the "after polishing" term M_a is subtracted from the "before polishing" term M_b

The resultant numerical term: material thickness removed (Δ^{m}) is accordingly divided by the process time Δ_t. This provides a semiconductor material thickness removal rate term within a numerical per second basis Δ_r.

$$\text{Material Removal Rate} = \Delta^m{}_r = (M_b - M_a)/\Delta_t$$

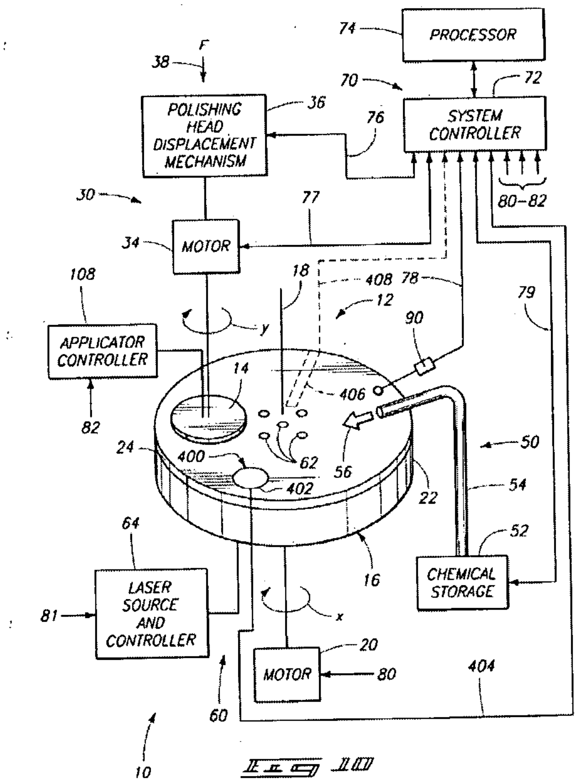
Please note that in col. 6, lines 50-65, Williams discloses that the thickness measurements of 10 previous wafers are then used to alter the polishing time of the next wafer to be polished.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the polishing method of Joslyn with a batch processing with end point detection as taught by Williams in order to alter the polishing time of the next wafer to be polished to improve the throughput of polishing process.

3. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joslyn'404 and Williams'549 as applied to claim 1 above, and further in view of Sandhu et al.'667.

Joslyn as modified by Williams has been discussed above, but the combination does not disclose the control of slurry feed rate in response to the change in polishing parameter.

With reference to Figure 10, col. 3, lines 30-54, Sandhu discloses an apparatus and method for polishing a wafer comprising a controller adjusting in situ slurry flow rate and temperature of wafer in response to the control information from the processor to effectuate a new polishing rate and a new polishing uniformity as the wafer polishing assembly continues to polish the face of the semiconductor wafer.



In accordance with one aspect of this invention, a system for polishing a semiconductor wafer comprises a wafer polishing assembly for polishing a face of a semiconductor wafer at a polishing rate and a polishing uniformity. The wafer polishing assembly has a plurality of controllable operational parameters that upon variation change the polishing rate and polishing uniformity. The system also comprises a controller operably coupled to the wafer polishing assembly for monitoring and managing in situ at least one of the operational parameters of the wafer polishing assembly. A processor is operably coupled to the controller for determining a set of desired operational parameters based on the monitored operational parameters and for outputting control information indicative of the desired operational parameters to the controller. The controller adjusts in situ at least one of the operational parameters of the wafer polishing assembly in response to the control information from the processor to effectuate a new polishing rate and a new polishing uniformity as the wafer polishing assembly continues to polish the face of the semiconductor wafer.

These operational parameters include platen rotational velocity, wafer rotational velocity, the polishing path of the wafer, the wafer speed across the platen, the down force exerted on the wafer, slurry composition, slurry flow rate, and temperature at the wafer surface.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the polishing method of Joslyn and Williams with a controller adjusting in situ slurry flow rate and temperature of wafer in response to the control information from the processor as taught by Sandhu in order to effectuate a new polishing rate and a new polishing uniformity as the wafer polishing assembly continues to polish the face of the semiconductor wafer. The advantage is to improve the throughput of polishing process.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yi et al.'949, Hempel et al.',950, Adams et al.'6,623,124, and

Shih et al.'535 all disclose a combined method of polishing a wafer with at least two different slurries.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Nguyen whose telephone number is 703-308-0163. The examiner can normally be reached on Monday-Friday/630AM-300PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Hail can be reached on 703-308-2687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Nguyen
Primary Examiner
Art Unit 3723

GEORGE NGUYEN
PRIMARY EXAMINER

GN – November 22, 2004